In the foregoing amendments, claims 1, 8, and 15 are amended. Claims 1-20 remain pending in the present application.

I.   Response to Objections to the Oath or Declaration

The oath or declaration was objected to as being defective because non-initialed and/or non-dated alterations were made therein. A substitute oath or declaration, without alterations, is submitted herewith and is believed to be proper in accordance with 37 CFR § 1.63. It is therefore respectfully requested that the Examiner enter the substitute oath or declaration and kindly withdraw the objection.

II.   Response to Objections to the Claims

Claims 1, 8, and 15 were objected to because of minor grammatical informalities. These informalities noted by the Examiner, and others, have been corrected by amendment herein. The amendments have been made as a matter of form to better define the invention and to make the claims more readable. The amendments have not been made for reasons related to patentability. Therefore no prosecution history estoppel arises from these amendments. *Black & Decker, Inc. v. Hoover Service Center* 886 F.2d 1285, 1294 n. 13 (Fed. Cir. 1989).

III.   Indication of Allowable Subject Matter

Applicant appreciates the Examiner's indication of allowable subject matter in the present application, in which claims 2-7, 9-14, and 16-20 would be allowable if re-written to include the subject matter of independent claims 1, 8, and 15 and any intervening claim. However, Applicant believes that independent claims 1, 8, and 15 are allowable in their present form and therefore chooses not to amend the claims according to the Examiner's suggestion at this time.

IV.   Response to 35 U.S.C. §102 Rejection

Claims 1, 8, and 15 stand rejected under 35 U.S.C. §102(e) as allegedly being anticipated by *Tiong et al.* (U.S. Patent No. 6,539,520). Applicant respectfully traverses this rejection on the grounds that *Tiong et al.* does not teach or disclose each and every element of the claims.

A. *Tiong et al.*

Tiong et al. is apparently directed to an Internet-based system for generating hardware description code. According to the abstract of *Tiong et al.*, the system includes a hardware description code generation "host" adapted to generate one or more hardware description language (HDL) files in response to one or more input parameters corresponding to a circuit. A user uploads the input parameters to the host and, in response, the host generates one or more HDL files.

Tiong et al. seems to make use of standard Internet protocols including TCP/IP and HTTP, which provides users access to files using HTML (col. 6, lines 47-54). The system 185 of *Tiong et al.* includes at least two entities, a user 190 and a hardware description code generator host 200, operatively interfacing with each other over the Internet 170' (col. 6, line 66 through col. 7, line 2). The user 190 desires to generate an HDL file that describes a circuit using the hardware description code generation host 200, typically for a fee (col. 7, lines 4-7).

The user 190 may upload input parameters 210 to the hardware description code generation host 200 and in response the hardware description code generation host 200 may generate an HDL file 220 using the input parameters 210 (col. 7, lines 12-15). The hardware description code generation host 200 provides a website that may include HTML forms for entering data, such as fill-in forms and/or pull down menus (col. 7, lines 26-30).

When the webpage 370 is displayed, users may enter one or more input parameters that describe the device, such as parameters that describe the ports of the device (col. 10, lines 8-10). The port type and name data provided by the user will cause the generation of a VERILOG netlist (col. 11, lines 1-3). The webpage 370' allows the user to enter port description parameters into the fields of an HTML input form 475 as values 440' or selected from a list in one or more pull down menus 480 (col. 11, lines 30-34). Using pull down menus 480", the user enters a particular feature of each port, such as the port name (col. 11, lines 58-64).

B. <u>Claim 1</u>

Independent claim 1 recites *"determining and storing a name for each joint test action group register...from said created flat netlist."* The Office Action seems to imply that *Tiong et al.* discloses all of the limitations of this claim, including

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"determining and storing a name...from said created flat netlist." Applicant respectfully disagrees with this conclusion and submits that *Tiong et al.* does not determine a name for each joint test action group (JTAG) register *"from said created flat netlist."* *Tiong et al.* actually discloses that the <u>user</u> enters port descriptions, including the "port name" (col. 11, lines 63-64). Since the user in *Tiong et al.* actually enters the port name, Applicant asserts that *Tiong et al.* fails to disclose that names for the JTAG registers are determined <u>from the netlist</u> as claimed.

Furthermore, claim 1 also recites *"determining relationships between each joint test action group register...and at least one input/output pin...from said created flat netlist."* The Office Action seems to suggest that *Tiong et al.* discloses this feature as well. However, Applicant disagrees with this suggestion because *Tiong et al.* actually discloses that the <u>user</u> enters the "input parameters that describe the device, such as parameters that describe the ports of the device" (*Tiong et al.* col. 10, lines 8-10). Although FIG. 3e of *Tiong et al.* illustrates a boundary scan chain with particular types of boundary scan cells and respective names, it should be noted that "the port type and name data [are] provided by the user" (col. 11, lines 1-2). In response to these entries by the <u>user</u> in the *Tiong et al.* reference, the netlist is then generated. Therefore, *Tiong et al.* fails to teach the claimed feature in which the netlist is created first and relationships between the JTAG registers and input/output pins are determined <u>from the netlist</u>.

C. <u>Claim 8</u>

Independent claim 8 recites *"means for determining and storing a name for each joint test action group register...from said created flat netlist."* The Office Action seems to imply that *Tiong et al.* discloses all of the limitations of the claims, even "means for determining and storing a name...from said created flat netlist." Applicant respectfully disagrees with this conclusion and submits that *Tiong et al.* does not provide structure for determining a name for each JTAG register *"from said created flat netlist."* *Tiong et al.* actually discloses that the <u>user</u> enters port descriptions, including the "port name" (col. 11, lines 63-64). Since the user in *Tiong et al.* enters the port name, Applicant asserts that *Tiong et al.* fails to disclose that names for the JTAG registers are determined <u>from the netlist</u> as claimed.

Claim 8 further recites *"means for determining relationships between each joint test action group register...and at least one input/output pin...from said created flat netlist."* The Office Action seems to suggest that *Tiong et al.* discloses this feature. However, Applicant traverses this suggestion since *Tiong et al.* actually discloses that the <u>user</u> enters the "input parameters that describe the device, such as parameters that describe the ports of the device" (col. 10, lines 8-10). Although FIG. 3e of *Tiong et al.* illustrates a boundary scan chain with particular types of boundary scan cells and respective names, it should be noted that *Tiong et al.* teaches that "the port type and name data [are] provided by the user" (col. 11, lines 1-2). In response to the user entering the port type and name data in *Tiong et al.*, the netlist is then generated from these entries. Therefore, *Tiong et al.* fails to teach the claimed feature in which the netlist is created and relationships between the JTAG registers and input/output pins are then determined <u>from the netlist</u>.

D.   <u>Claim 15</u>

Independent claim 15 is directed to a system for generating a boundary-scan description language file for an integrated circuit. The system includes a processor that performs a step of *"determining and storing a name for each joint test action group register...from said created flat netlist."* The Office Action seems to imply that *Tiong et al.* discloses all of the limitations of the claims, including a processor that perform the step of "determining and storing a name...from said created flat netlist." Applicant respectfully disagrees with this conclusion and submits that *Tiong et al.* does not determine a name for each joint test action group register *"from said created flat netlist"* as claimed. *Tiong et al.* actually discloses that the <u>user</u> enters port descriptions, such as the "port name" (col. 11, lines 63-64). Since the <u>user</u> in *Tiong et al.* actually enters the port name, Applicant asserts that *Tiong et al.* fails to disclose that names for the JTAG registers are determined <u>from the netlist</u> as claimed.

Furthermore, the processor of claim 15 also performs *"determining relationships between each joint test action group register...and at least one input/output pin...from said created flat netlist."* The Office Action seems to suggest that *Tiong et al.* discloses this feature as well. Applicant disagrees with this suggestion. Actually, *Tiong et al.* discloses that the <u>user</u> enters the "input parameters that describe the device, such as parameters that describe the ports of the device" (col.

10, lines 8-10). Although FIG. 3e of *Tiong et al.* illustrates a boundary scan chain with particular types of boundary scan cells and respective names, it should be noted that *Tiong's* "port type and name data [are] provided by the user" (col. 11, lines 1-2). In response to these entries by the user in *Tiong et al.*, the netlist is then generated. Therefore, *Tiong et al.* fails to teach the claimed feature in which the netlist is created first and relationships between the JTAG registers and input/output pins are determined from the netlist.

For at least these reasons, it is respectfully submitted that *Tiong et al.* fails to meet the criteria for establishing a *prima facie* case of anticipation of claims 1, 8, and 15. Therefore, the Applicant requests that the Examiner kindly withdraw the rejection of these claims.
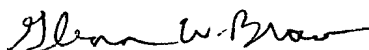
V.   Prior Art

The prior art made of record has been considered, but is not believed to affect the patentability of the presently pending claims.

CONCLUSION

In light of the foregoing amendments and for at least the reasons set forth above, Applicant respectfully submits that all objections and/or rejections have been traversed and/or accommodated, and that pending claims 1-20 are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned at (770) 933-9500.

Respectfully submitted,

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THOMAS, KAYDEN,
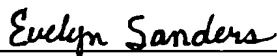 **HORSTEMEYER & RISLEY, L.L.P.**
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on 11/24/2003.

Signature – Evelyn Sanders

Attachment(s):   Substitute Oath or Declaration